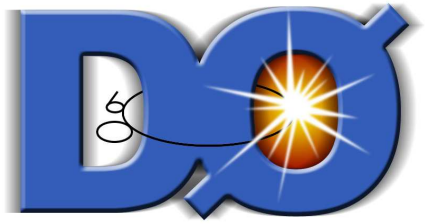
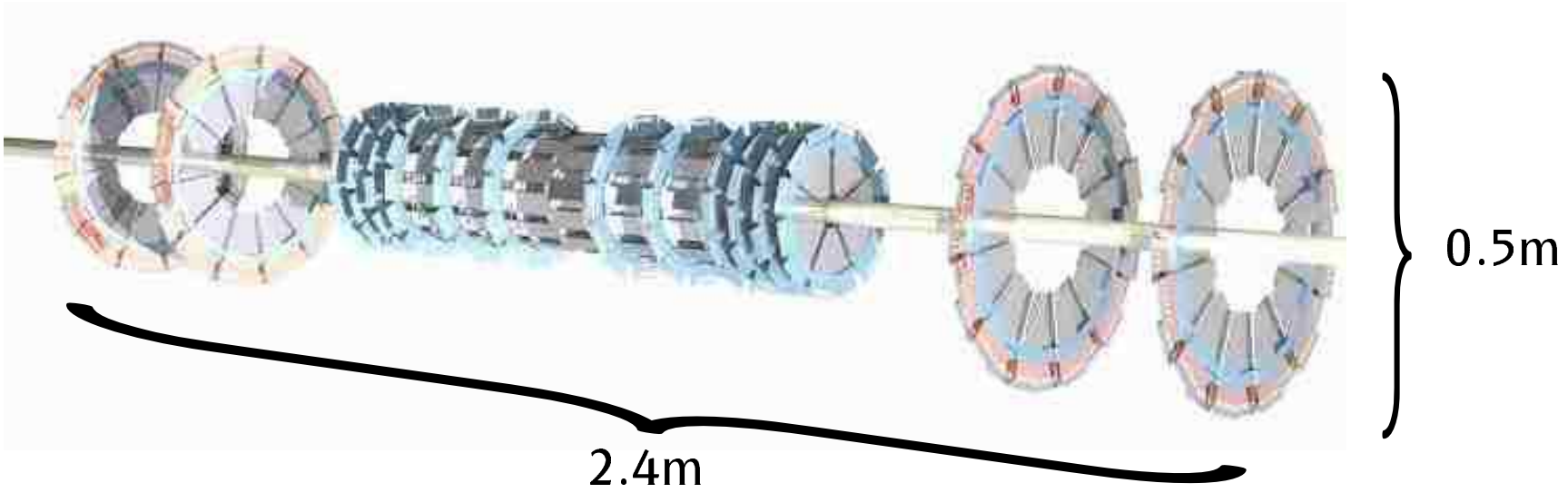


APS April Meeting 2004, Denver, 2 May 2004

Electrical Characterization of Silicon Readout Modules for the DØ Upgrade

Kristian Harder, Kansas State University,
for the DØ Collaboration

the current DØ silicon vertex detector



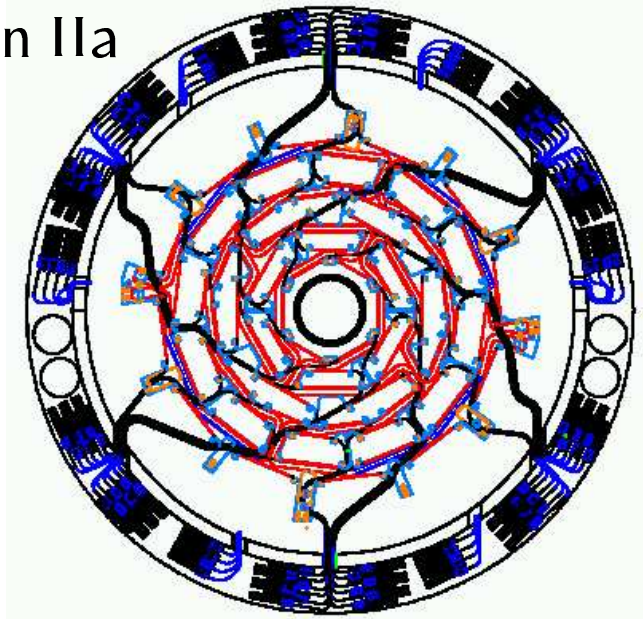
- 6 barrel modules à 4 superlayers
- 16 disks for forward tracking

good detector, but

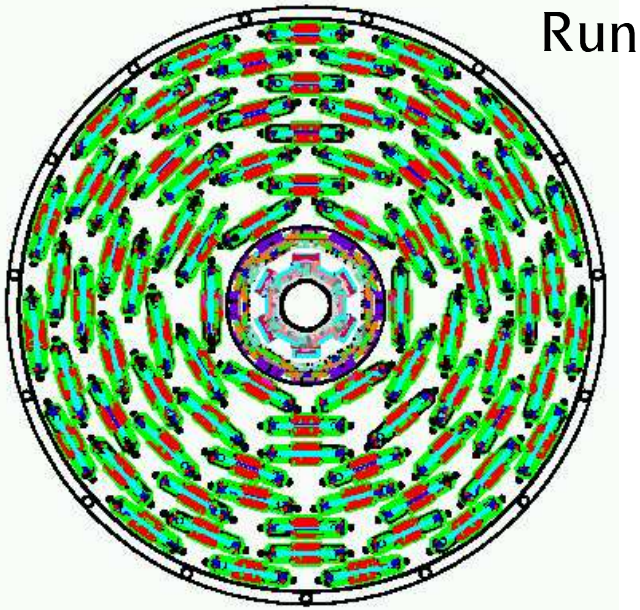
- severe radiation damage expected after $\approx 4\,\mathrm{fb}^{-1}$
- complex design $\longrightarrow$ harder to build, maintain, understand

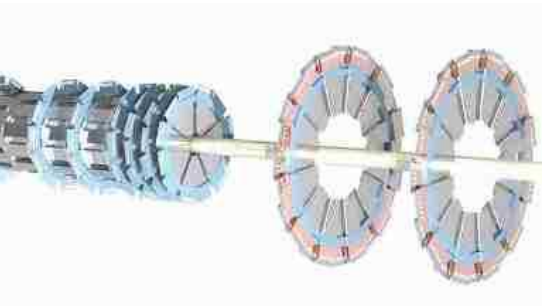
DØ Run IIb silicon upgrade

Run IIa

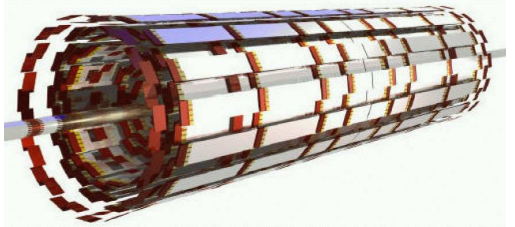


Run IIb





- barrels only, no disks
- simpler cabling
- 6 superlayers instead of 4
- larger radial coverage
- only single-sided detectors



much simpler, much more robust design!

only one disadvantage….

...it will not be built!

silicon detector replacement for Run IIb cancelled due to
- Tevatron performance
- budget issues

instead: add layer 0 to current detector (see next talk)

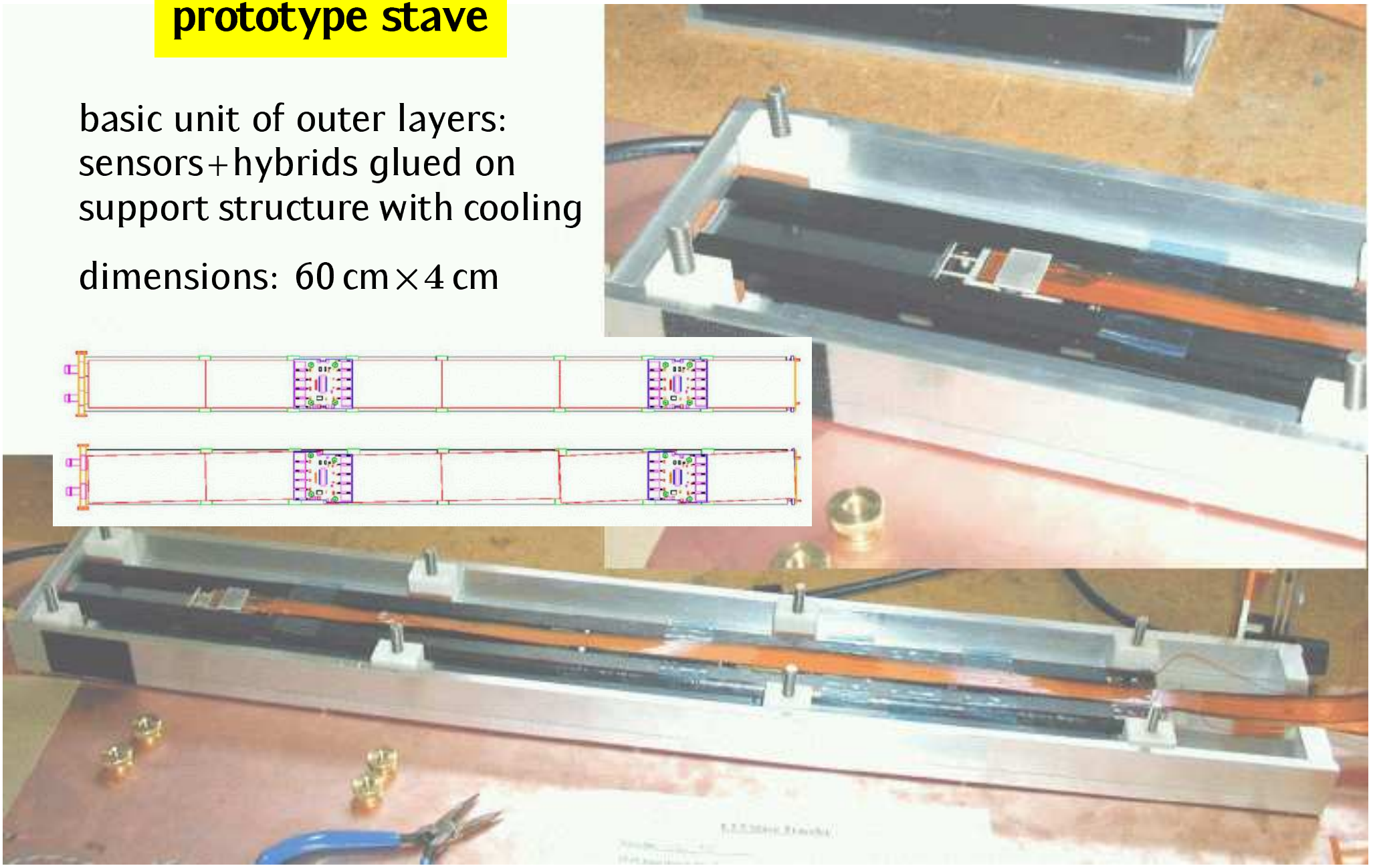
we do profit from the work done so far:
- layer 0 builds on it
- better understanding of (+new experts for) current detector
- point to start from for other projects?

 definitely worth showing the prototype test results!

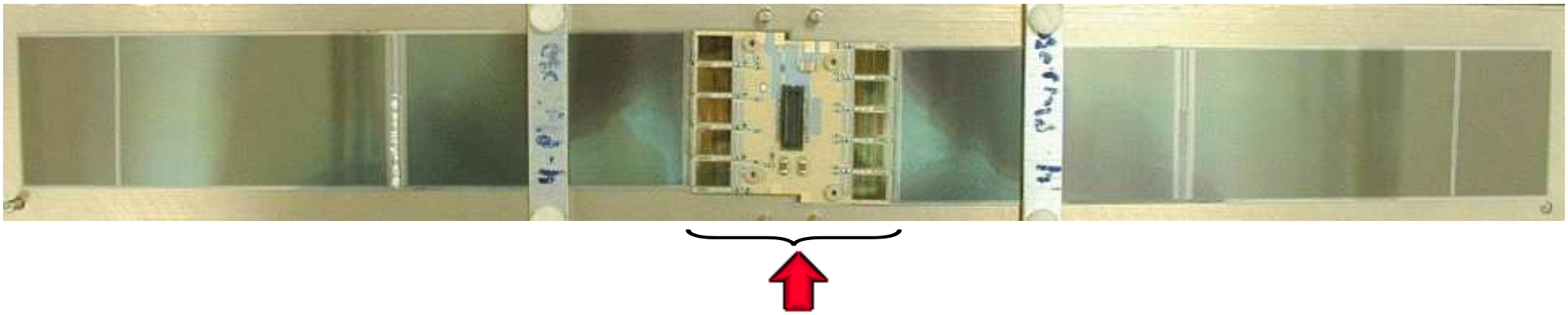
prototype stave

basic unit of outer layers:
sensors+hybrids glued on
support structure with cooling

dimensions: $60\,\text{cm} \times 4\,\text{cm}$



detector readout

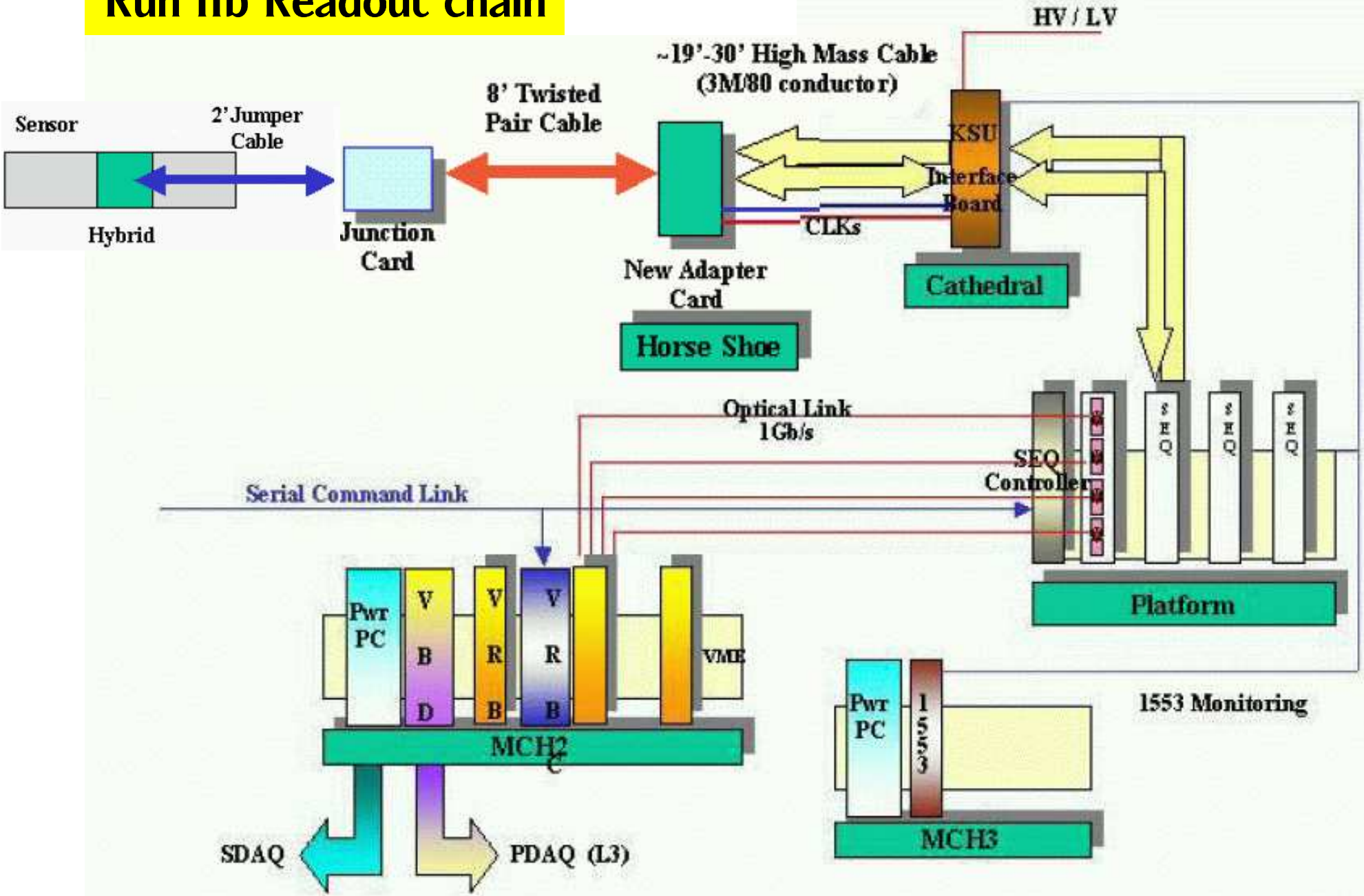


readout hybrids = SVX4 readout chips on beryllium substrate

SVX4 chips:

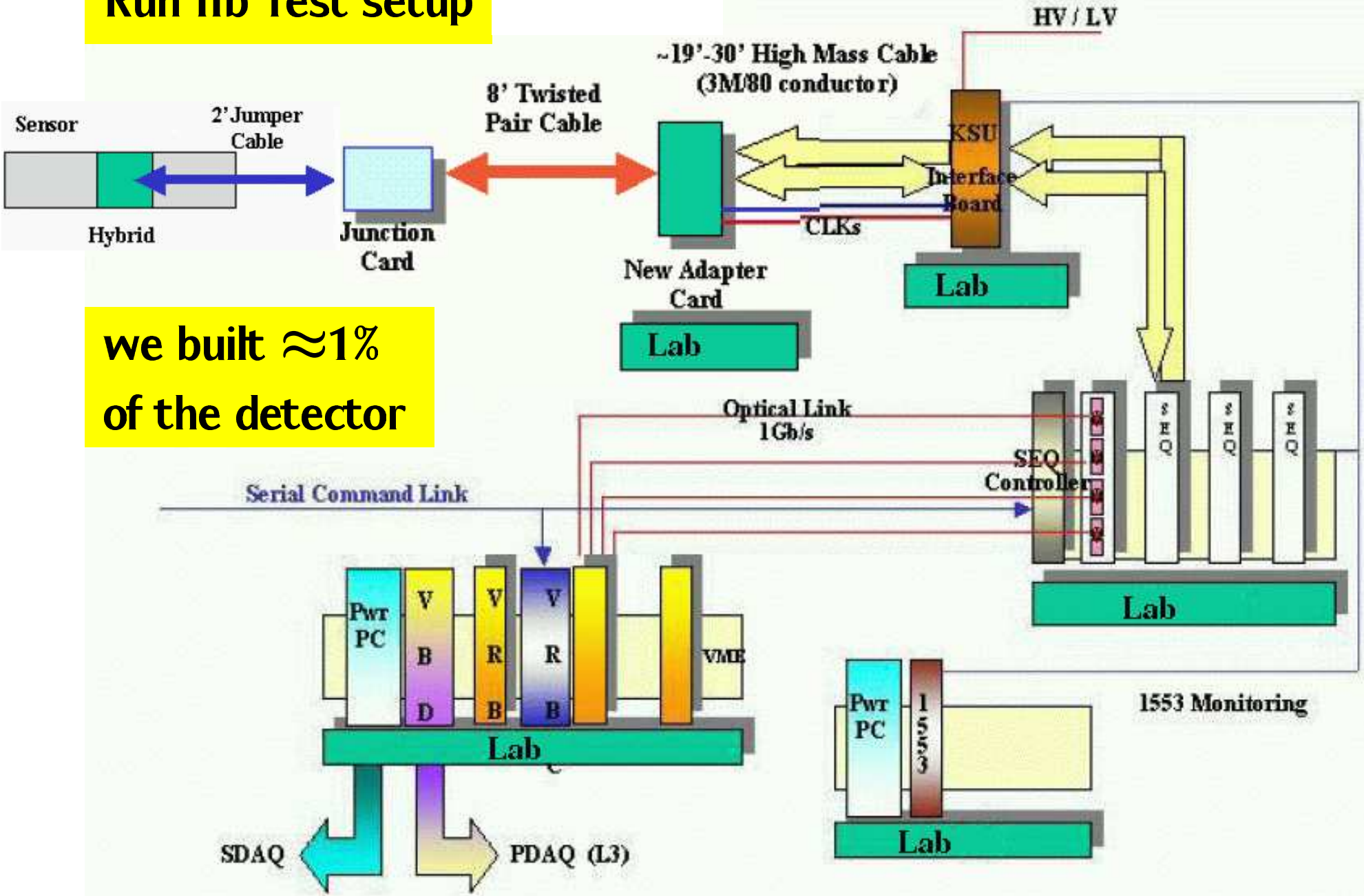
- based on SVX2, SVX3 chips in use at DØ , CDF
- 128 channels per chip
- daisy-chained operation → less cabling
- differential data signals → less noise
- readout sparsification: read only channels above threshold
- can inject calibration charge into any pattern of channels

Run IIb Readout chain



Run IIb Test setup

we built ≈1%
of the detector



Goals of electrical characterization

Does it work at all?

communication between the components

Can we actually see something?

noise level

Do we see what we expect to see?

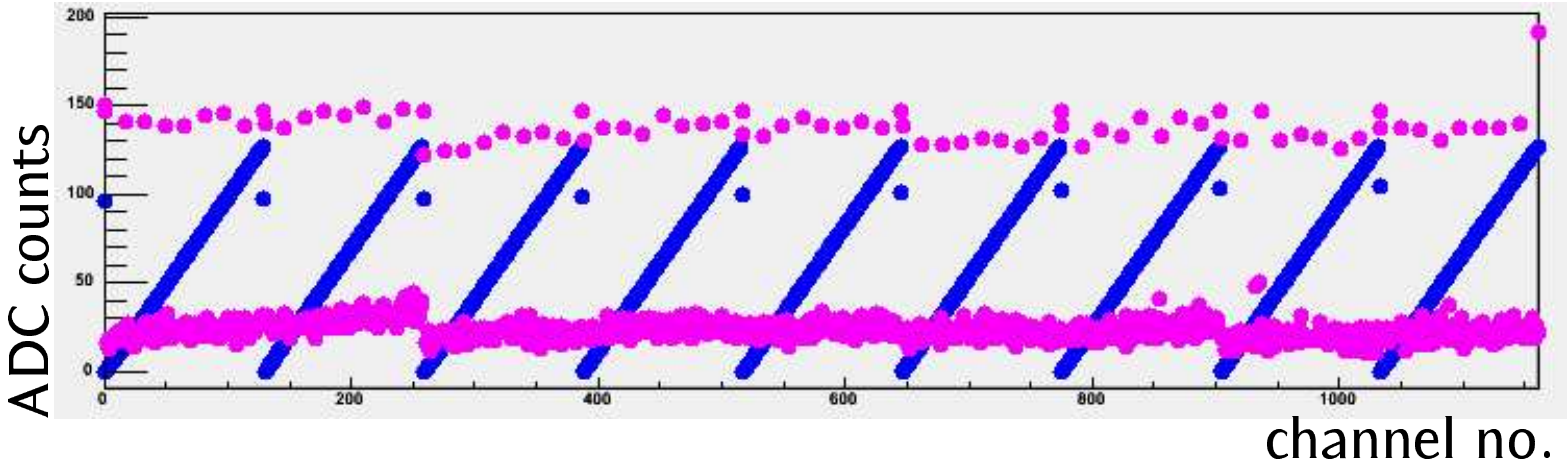
timing, …

Let's go through some examples

some of them obtained with simpler test setups

Data integrity I

simple test for data integrity: read all channels



easy to verify data integrity:
for each chip

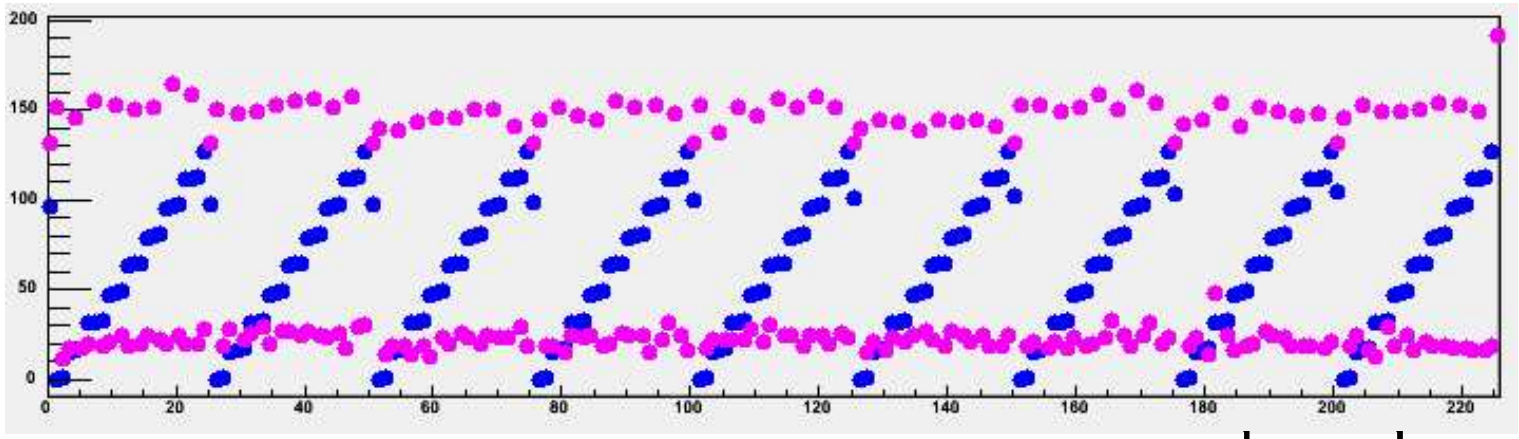
- expect chip ID
- expect 128× channel ID + data
- know exactly which channel IDs to expect

millions of events without errors!

tests with realistic trigger rates done

Data integrity II

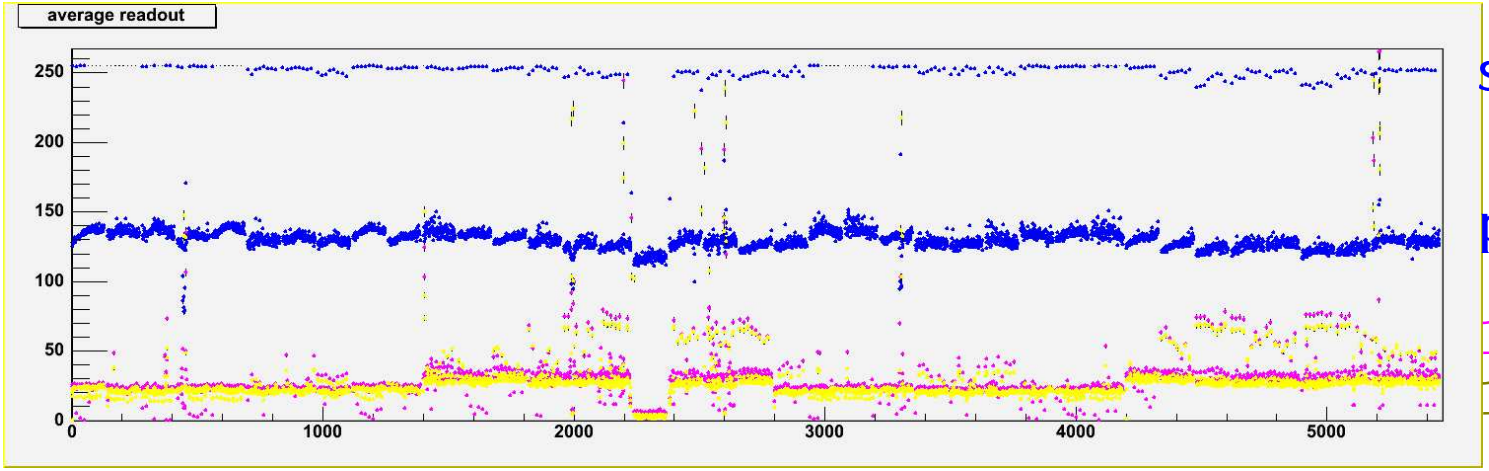
realistic mode: read only channels above threshold + neighbors



error checking requires sophisticated algorithms,
some failure modes can not be identified
error discovery efficiency tuned with MC simulation

again, our prototypes show excellent performance!

Noise performance

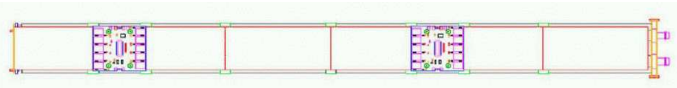


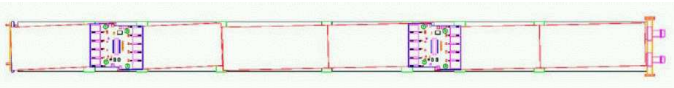
signal

pedestal

$10\times$ total noise

$10\times$ incoh. noise

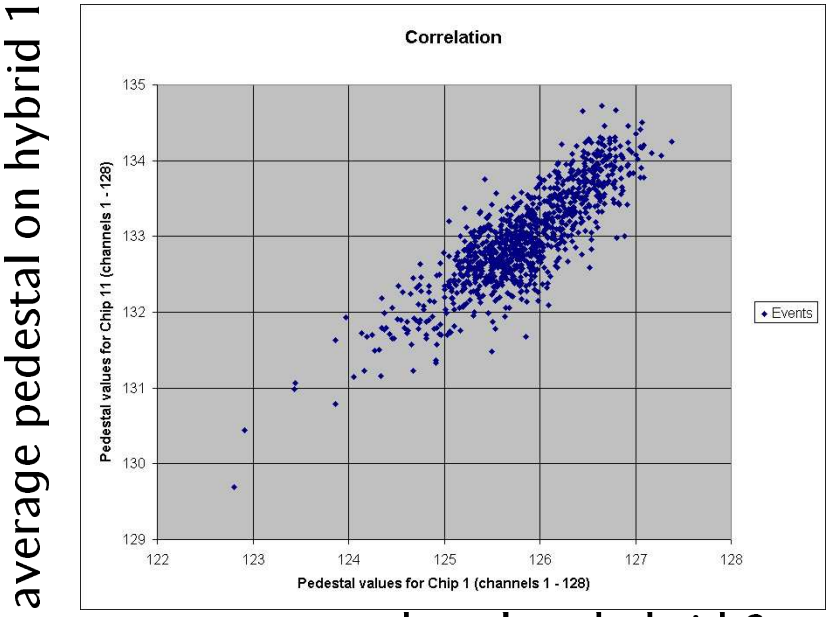




noise as expected, generally below 3–4 ADC counts
$\longrightarrow$ signal to noise ratio: $\approx$ 10–12
same noise level in sparse readout mode

Timing verification

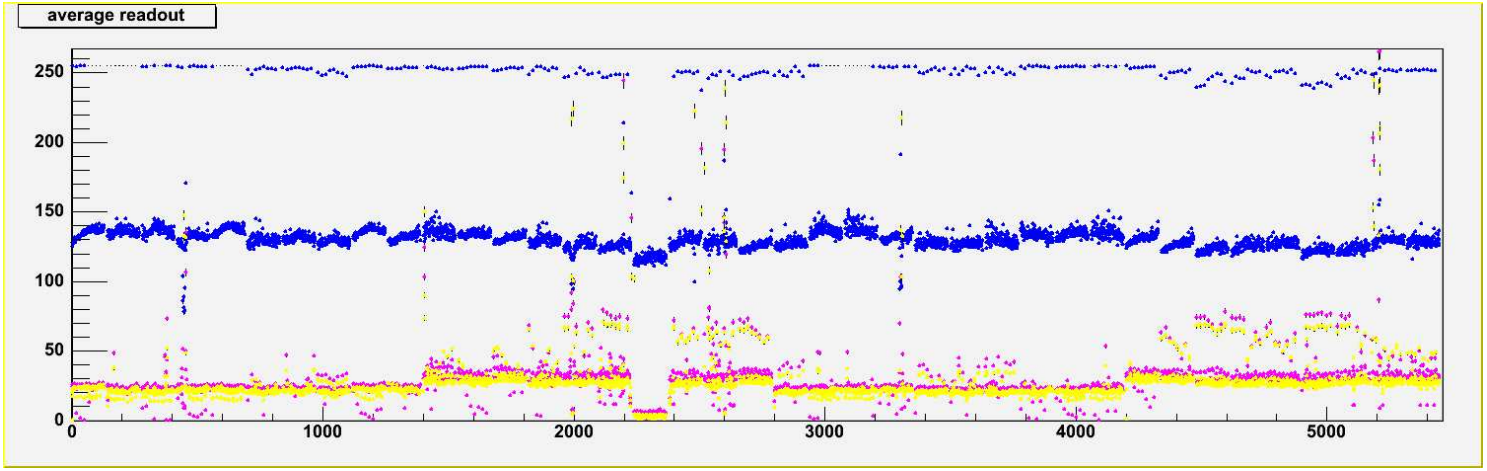
SVX chips store signals in pipeline
do we access the correct pipeline cell during readout?
are we reading all modules at the same time?
➡ exploit coherent noise for verification



average pedestal on hybrid 1

average pedestal on hybrid 2

Prototype stave: summary



excellent performance, all specifications met

specific problems as evident in the plot above:

- one dead chip
- a few noisy channels (pinholes)
- noise pickup in charge injected channels
- pedestal spread & structures (fixed by new SVX4 revision)

Plans

construct final prototype with new SVX4 version

document everything

build layer 0